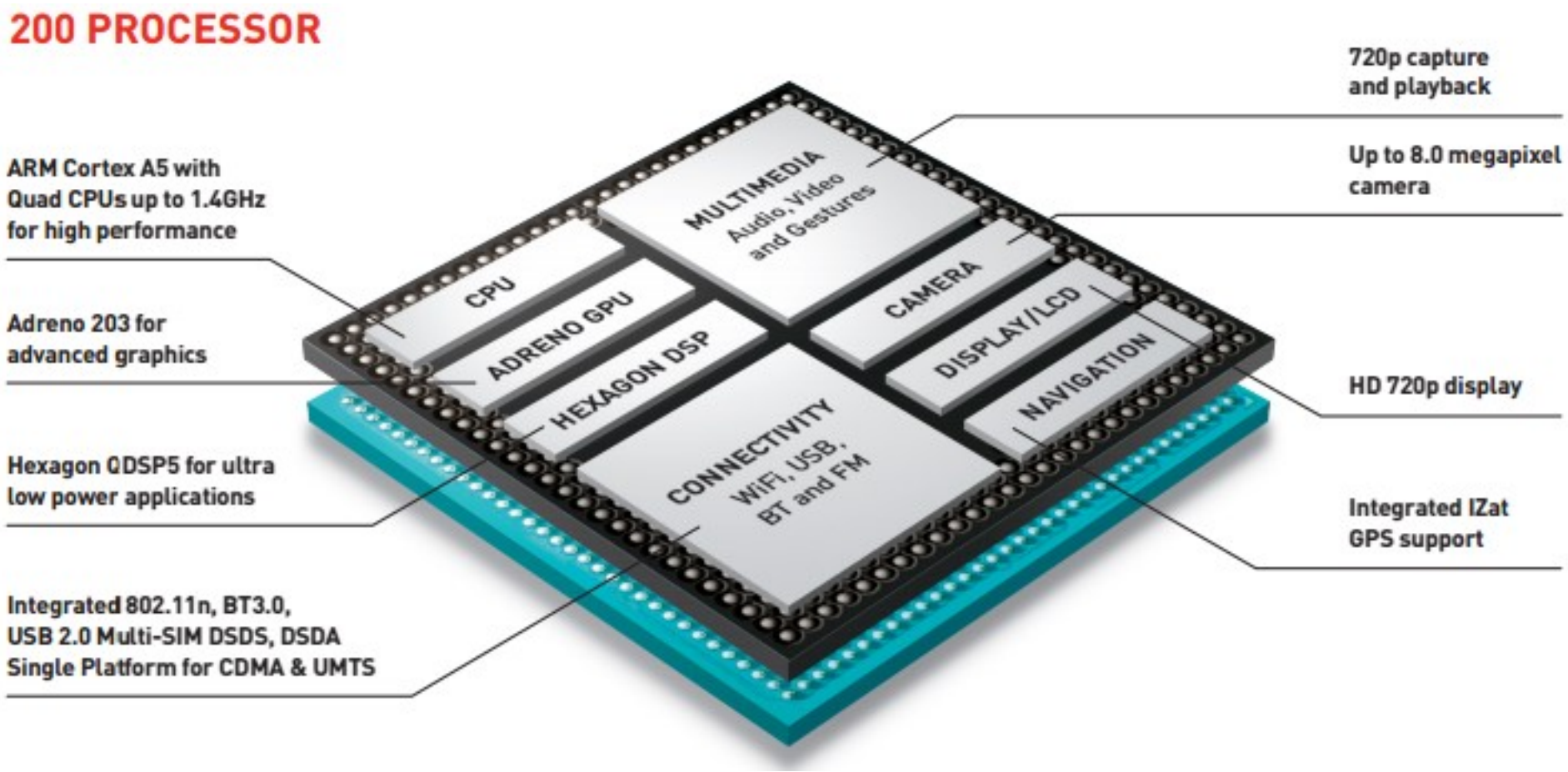
On-chip Peripherals

EE5182 Microcontrollers and Embedded Systems

System on a Chip (SoC)

- All the necessary components of a computer system are embedded on a single silicon die.
- A typical SoC will contain:
  - A processor
  - Onboard execution memory (SRAM)
  - Many microcontrollers may contain FLASH memory for program storage
  - Peripheral systems and interfaces connected to the processing core via a SoC bus

System on a Chip (SoC)



SoC Design

- IP hardware blocks and software blocks developed in parallel
- Hardware in CAD
- Software in development environment
- Emulated and verified on FPGA (field-programmable gate arrays)
- Place and Route, created in silicon

SoC Advantages

- Decreased power consumption
- Increased reliability
- Smaller board space
- Can be cheaper when using ready to go components

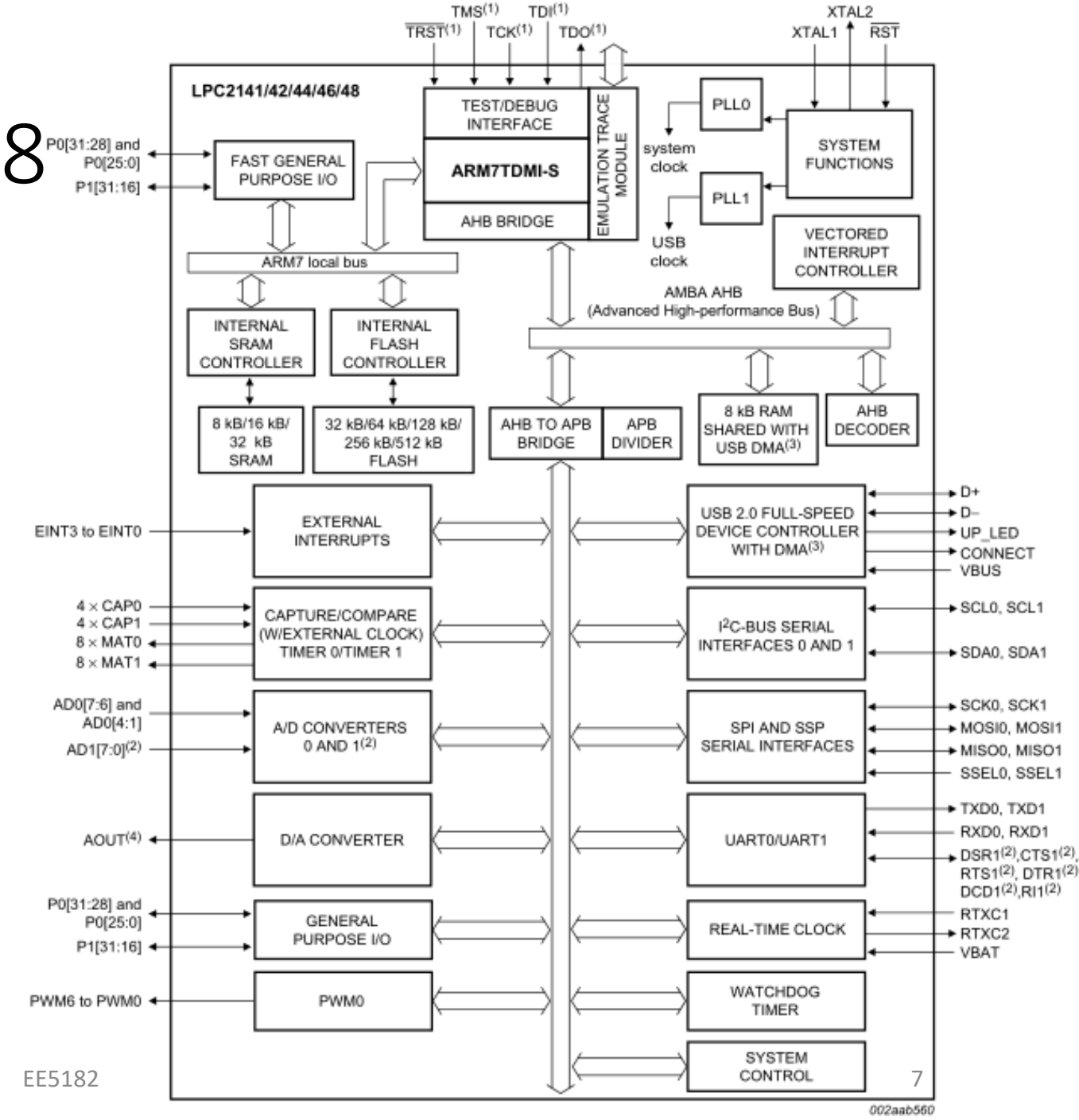
- More tightly integrates SoCs will result in smaller electronic products that use less power, are faster, and more reliable
- Nano scale robots for fighting human diseases, curing diseases.

SoC Disadvantages

- Extremely high design cost (for the actual chip)
- Large silicon space may be required
- Component testing may be difficult
- Prototyping may take longer
- Intellectual property (IP) issues

SoC Example: LPC2148

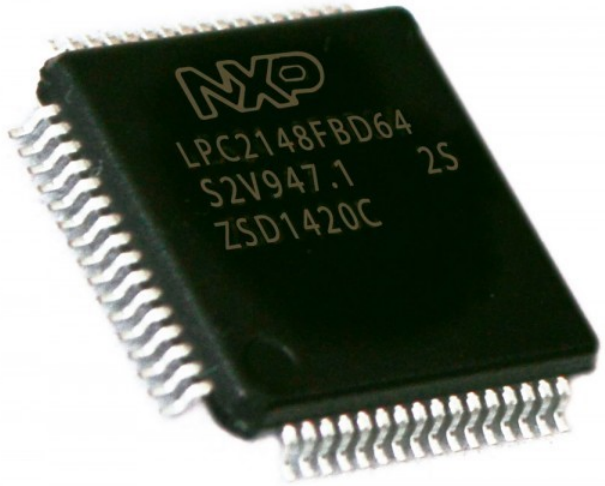
- LPC2148 is the widely used IC from ARM-7 family manufactured by Philips.
- It is pre-loaded with many inbuilt peripherals making it more efficient and a reliable option.
- Single-chip 32-bit RISC microcontroller, with 512 kB flash ROM and 32KB RAM.



On-chip Peripherals

- On-chip flash program memory
- On-chip static RAM
- Interrupt controller
- General purpose timers/external event counters
- Watchdog timer
- Real-time clock
- Pulse width modulator
- Fast general purpose parallel I/O
- ADC
- DAC
- USB
- UARTs
- I2C
- SPI
- SSP

On-chip Peripherals: LPC2148



- Key features:
  - In-System Programming (ISP) and In-Application Programming (IAP)
  - Vectored Interrupt Controller
  - Two 10bit ADCs with 14 channels
  - USB 2.0 Full Speed Device Controller
  - Two UARTs, one with full modem interface
  - Two I2C serial interfaces
  - Two SPI serial interfaces
  - Two 32-bit timers
  - Watchdog Timer
  - PWM unit
  - Real Time Clock with optional battery backup
  - Brown out detect circuit General purpose I/O pins
  - CPU clock up to 60 MHz
  - On-chip crystal oscillator and On-chip PLL

On-chip flash program memory

- LPC2148 incorporates a 512 kB flash memory system.
- This memory may be used for both code and data storage.
- Programming of the flash memory may be accomplished in several ways.
- It may be programmed In System via the serial port.
- The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc.
- Due to the architectural solution chosen for an on-chip boot loader, flash memory available for user's code on LPC2148 is 500 kB.
- The LPC2148 flash memory provides a minimum of 100 000 erase/write cycles and 20 years of data-retention.

On-chip static RAM

- On-chip static RAM may be used for code and/or data storage.
- The SRAM may be accessed as 8-bit, 16-bit, and 32-bit.
- The LPC2148 provides 32 kB of static RAM.
- In case of LPC2148, an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

Interrupt controller

- The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as:
  - Fast Interrupt reQuest (FIQ)
  - Vectored Interrupt ReQuest (IRQ)
  - Non-vectored IRQ.
- The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

Interrupt controller

- The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor.
- Interrupt sources:
  - Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags.
  - Individual interrupt flags may also represent more than one interrupt source.

Pin connect block

- The pin connect block allows selected pins of the microcontroller to have more than one function.
- Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals.
- Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled.
- Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.
- The Pin Control Module with its pin select registers defines the functionality of the microcontroller in a given hardware environment.

Fast general purpose parallel I/O (GPIO)

- Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers.
- Pins may be dynamically configured as inputs or outputs.
- Separate registers allow setting or clearing any number of outputs simultaneously.
- The value of the output register may be read back, as well as the current state of the port pins.

Fast general purpose parallel I/O (GPIO)

- LPC2148 introduced accelerated GPIO functions.
  - GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte addressable.
  - Entire port value can be written in one instruction.
- Features
  - Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
  - Direction control of individual bits.
  - Separate control of output set and clear.
  - All I/O default to inputs after reset.

10-bit ADC

- The LPC2148 contain two analog to digital converters.
- These converters are single 10-bit successive approximation analog to digital converters.
- While ADC0 has six channels, ADC1 has eight channels.
- Therefore, total number of available ADC inputs for LPC2148 is 14.

10-bit ADC

- Features
  - 10 bit successive approximation analog to digital converter.
  - Each converter capable of performing more than 400000 10-bit samples per second.
  - Every analog input has a dedicated result register to reduce interrupt overhead.
  - Burst conversion mode for single or multiple inputs.
  - Optional conversion on transition on input pin or timer match signal.
  - Global Start command for both converters.

10-bit DAC

- The DAC enables the LPC2148 to generate a variable analog output.
- The maximum DAC output voltage is the VREF voltage.
- Features
  - 10-bit DAC.
  - Buffered output.
  - Power-down mode available.
  - Selectable speed versus power.

USB 2.0 device controller

- The USB is a 4-wire serial bus that supports communication between a host and a number (127 max) of peripherals.
- The host controller allocates the USB bandwidth to attached devices through a token based protocol.
- The bus supports hot plugging, unplugging, and dynamic configuration of the devices.
- All transactions are initiated by the host controller.

USB 2.0 device controller

- The LPC2148 is equipped with a USB device controller that enables 12 Mbit/s data exchange with a USB host controller.
- It consists of a register interface, serial interface engine, endpoint buffer memory and DMA controller.
- The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory.
- The status of a completed USB transfer or error condition is indicated via status registers.
- An interrupt is also generated if enabled.

UARTs

- The LPC2148 contains two UARTs.
- In addition to standard transmit and receive data lines, the LPC2148 UART1 also provides a full modem control handshake interface.
- UARTs in LPC2148 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 with any crystal frequency above 2 MHz.
- In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

UARTs

- Features
  - 16 B Receive and Transmit FIFOs.
  - Register locations conform to 16C550 industry standard.
  - Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
  - Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
  - Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
  - LPC2144/46/48 UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

I^2C-bus serial I/O controller

- The LPC2148 each contains two I^2C-bus controllers.
- The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial DAta line (SDA).
- Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)).
- Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed.
- The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.
- The I^2C-bus implemented in LPC2148 supports bit rates up to 400 kbit/s (Fast I^2C-bus).

SPI serial I/O controller

- The LPC2148 each contains one (Serial Peripheral Interface) SPI controller.
- The SPI is a full duplex serial interface, designed to handle multiple masters and slaves connected to a given bus.
- Only a single master and a single slave can communicate on the interface during a given data transfer.
- During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

SSP serial I/O controller

- The LPC2148 each contains one Serial Synchronous Port controller (SSP).
- The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus.
- It can interact with multiple masters and slaves on the bus.
- However, only a single master and a single slave can communicate on the bus during a given data transfer.
- The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master.

General purpose timers/external event counters

- The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers.
- It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.
- Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

Watchdog timer

- The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state.
- When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

Real-time clock

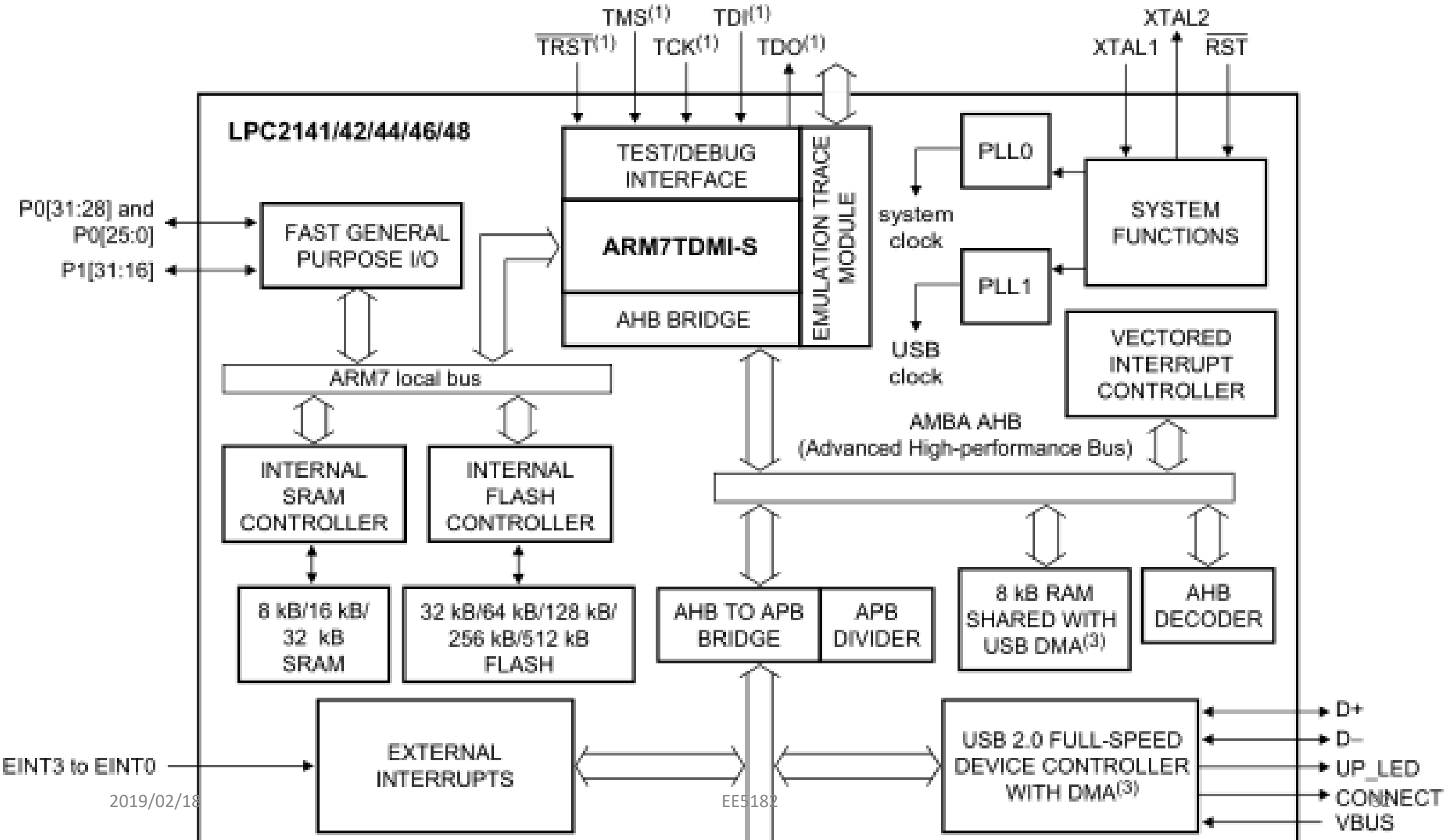
- The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected.
- The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

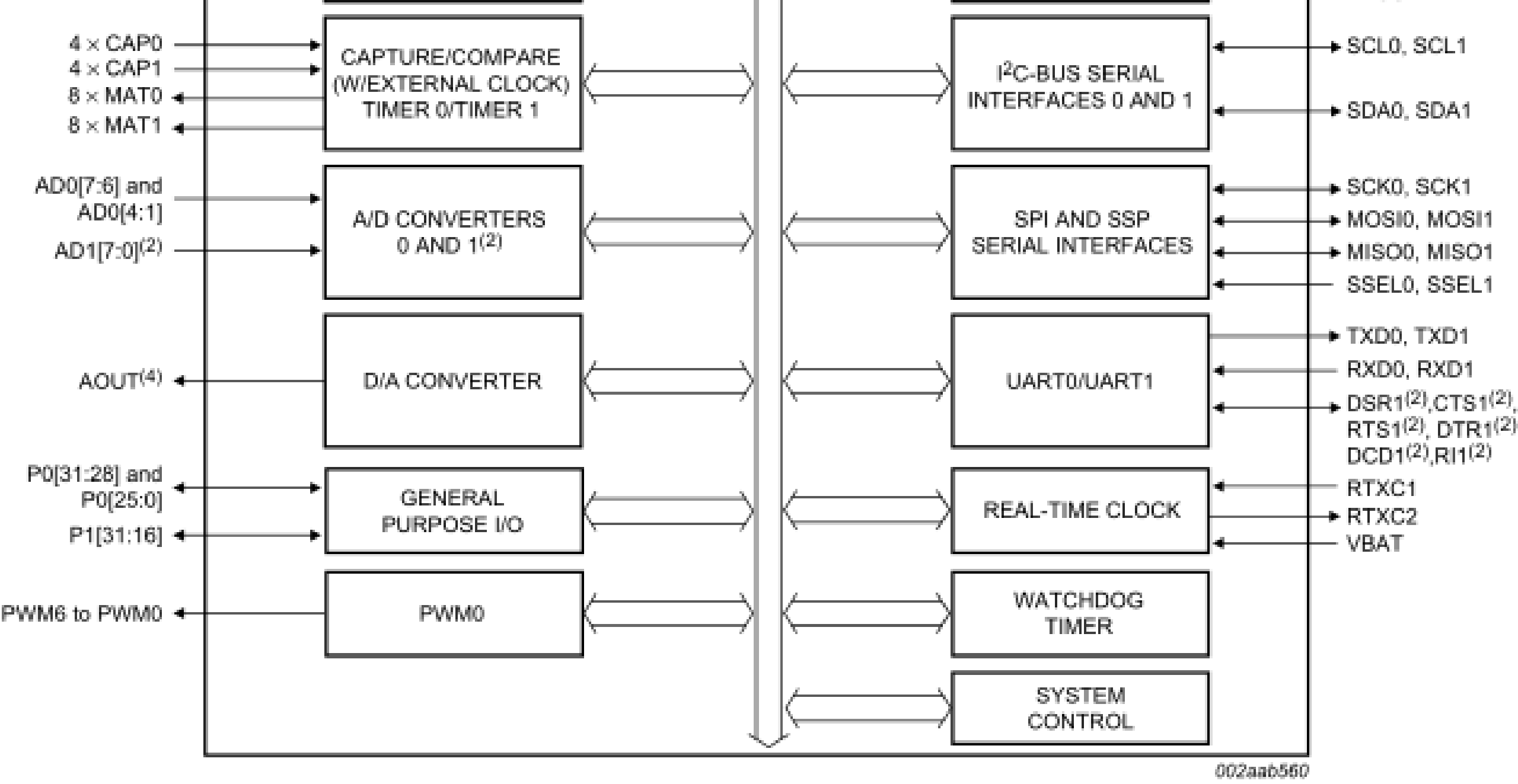
Pulse width modulator

- The PWM is based on the standard timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2148.
- The timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers.
- The ability to separately control rising and falling edge locations allows the PWM to be used for more applications.
- For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

System control

- Crystal oscillator
- PLL (phase-locked loop)
- Reset and wake-up timer
- Brownout detector
- Code security
- External interrupt inputs
- Memory mapping control
- Power control
- APB bus


LPC2141/42/44/46/48
TMS(1)
TDI(1)
TRST(1)
TCK(1)
TDO(1)
XTAL2
XTAL1
RST
TEST/DEBUG INTERFACE
ARM7TDMI-S
AHB BRIDGE
EMULATION TRACE MODULE
PLL0
PLL1
SYSTEM FUNCTIONS
system clock
USB clock
P0[31:28] and P0[25:0]
P1[31:16]
FAST GENERAL PURPOSE I/O
ARM7 local bus
VECTORED INTERRUPT CONTROLLER
AMBA AHB (Advanced High-performance Bus)
INTERNAL SRAM CONTROLLER
INTERNAL FLASH CONTROLLER
8 kB/16 kB/ 32 kB SRAM
32 kB/64 kB/128 kB/ 256 kB/512 kB FLASH
AHB TO APB BRIDGE
APB DIVIDER
8 kB RAM SHARED WITH USB DMA(3)
AHB DECODER
EINT3 to EINT0
EXTERNAL INTERRUPTS
USB 2.0 FULL-SPEED DEVICE CONTROLLER WITH DMA(3)
D+
D–
UP_LED
CONNECT
VBUS


4 × CAP0
4 × CAP1
8 × MAT0
8 × MAT1
CAPTURE/COMPARE (W/EXTERNAL CLOCK) TIMER 0/TIMER 1
I2C-BUS SERIAL INTERFACES 0 AND 1
SCL0, SCL1
SDA0, SDA1
AD0[7:6] and AD0[4:1]
AD1[7:0](2)
A/D CONVERTERS 0 AND 1(2)
SPI AND SSP SERIAL INTERFACES
SCK0, SCK1
MOSI0, MOSI1
MISO0, MISO1
SSEL0, SSEL1
AOUT(4)
D/A CONVERTER
UART0/UART1
TXD0, TXD1
RXD0, RXD1
DSR1(2),CTS1(2), RTS1(2), DTR1(2) DCD1(2),RI1(2)
P0[31:28] and P0[25:0]
P1[31:16]
GENERAL PURPOSE I/O
REAL-TIME CLOCK
RTXC1
RTXC2
VBAT
PWM6 to PWM0
PWM0
WATCHDOG TIMER
SYSTEM CONTROL
002aab560

Reference

- https://www.nxp.com/docs/en/data-sheet/LPC2141_42_44_46_48.pdf